Disadvantage of On-chip Transient Protection

Relying upon on-chip protection to suppress ESD/EOS events may provide a false sense of security if not carefully evaluated. In the past, 2kV-4kV of on-chip ESD protection was thought to be adequate protection. New standards such as IEC 61000-4-2 have raised the minimum protection level to as much as 15kV. As device geometries continue to shrink, it is becoming more difficult to add on-chip protection with a common manufacturing process. As a result, devices operating at low voltages may not be adequately protected. This application note will discuss the disadvantages of on-chip protection and provide the designer with applications information for adding external protection components to insure maximum ESD/EOS immunity.

Typical CMOS input protection

Some integrated circuits feature built in protection by means of an internal SCR or resistor and diode network. The basic requirements of a protection network are that it provide a low impedance path for the discharge energy while limiting the current and voltage seen by the active circuit. This means that the transient energy is dissipated in the transceiver itself. The basic input protection circuit usually consists of the following elements:

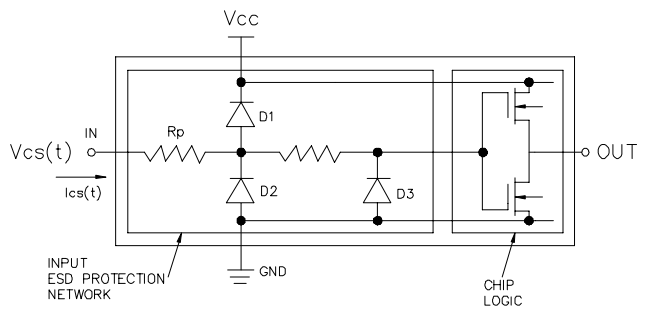

Figure 1 - Typical CMOS Input Protection Scheme

- A shunt device to discharge positive polarity transients
- A shunt device to discharge negative polarity transients
- A series element for current limiting

A typical CMOS input protection circuit is shown in Figure 1. When an ESD voltage is applied to the input

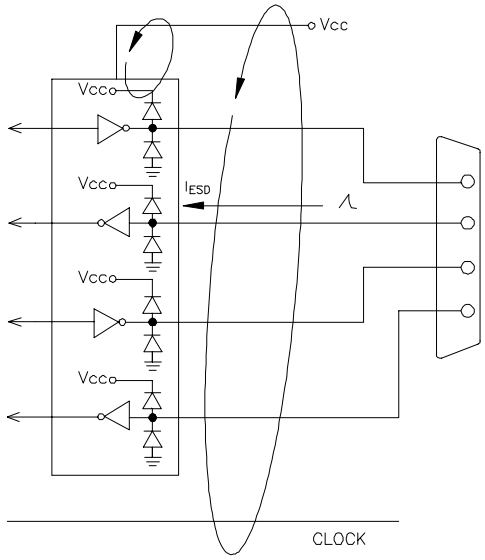

Figure 2a - IC with Internal ESD Protection

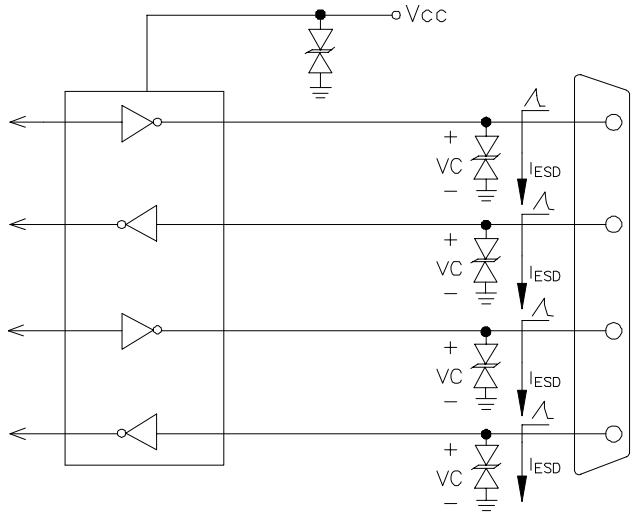

Figure 2b - TVS Diode Protection Points

structure, the on-chip diodes shunt the transient current to the power line (VCC) or ground. A positive transient voltage causes diode D1 to be forward biased when the input voltage exceeds VCC. Likewise, for negative transients, Diode D2 shunts the negative current. The polysilicon input resistors serve to limit the peak currents. Since polysilicon resistors are thermally insulated by a surrounding layer of SiO_2 or glass they are particularly susceptible to thermal damage resulting from joule heating by ESD induced currents. A typical CMOS input protection circuit can provide ESD immunity to approximately 4kV.

Alternative Protection Schemes

On-chip protection should be viewed as a secondary measure only and should not be relied upon as the sole protection method. The first reason is that placement of the protection element is critical. ESD induced transients can be coupled into nearby traces including data lines, clock signal lines, and power supply rails (Figure 2a). Additionally, the magnitude of the voltage across the chip is increased due to Ldi/dt effect and can exceed the capability of the input protection network (Vpk = VESD + Ldi/dt). *External protection elements designed to absorb high levels of transient energy are normally required to provide reliable ESD/EOS protection, even if the protected device includes some form of on-chip protection*. For protection of data and I/O ports, the external protection element should be placed near the signal entry point. By diverting the transient to ground immediately, radiation to nearby circuitry is reduced (Figure 2b). While many devices may offer protection for ESD induced transients, they offer little or no protection for longer duration pulses such as those associated with lightning. This is especially critical for equipment with outside line connections such as point-of-sale systems and cellular base stations.

Design Example

Figure 3 illustrates how to protect a typical 3 x 5 RS-232 Driver/Receiver (NSC DS14185) using Semtech's SMDA24C-8 TVS array. The SMDA24C-8 is designed to protect 8 bidirectional I/O lines operating at 12V. The DS14185 transceiver has internal ESD protection to 2.5kV. The addition of the SMDA24C-8 increases the ESD protection to >15kV. This combination offers a low cost, high reliability solution to aid in meeting the requirements of IEC 61000-4-2. As always, ESD/EOS

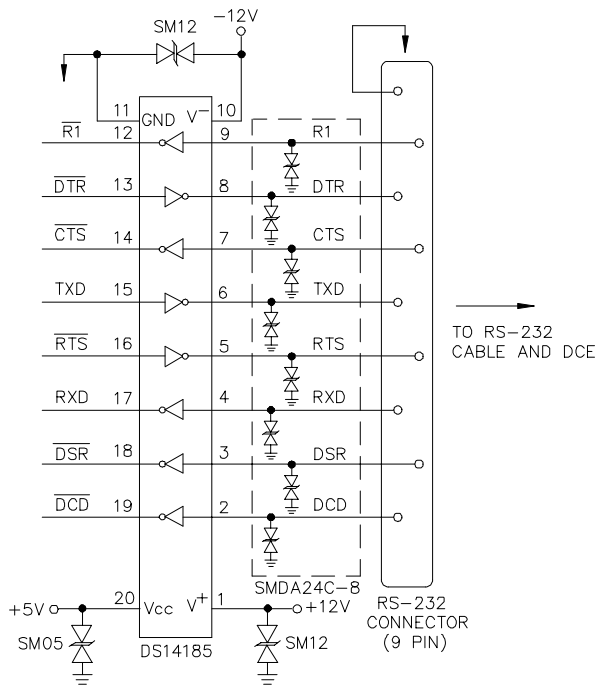

Figure 3 - RS-232 Design Example

protection is recommended at the power supply rails as well as the I/O interface. Semtech SM05 and SM12 are used to protect the 5V and 12V supplies respectively. Finally, while TVS diodes are necessary for suppression of conducted transients, good pc board layout and equipment shielding is required to guard against electromagnetic coupling and externally radiated events.

References:

1 Greason, William D., "*Electrostatic Damage in Electronics: Devices and Systems*", Research Studies Press Ltd., 1989.
2 Russell, William, "*Protecting Portable Devices from ESD Damage*", Communications Systems Design Magazine, April, 1997
3 National Semiconductor Corporation, Interface Products Databook, 1996